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2. Patent application number

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9913326.6

3. Full name, address and postcode of the or of each applicant (underline all surnames)

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1000 AZTEC WEST
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Patents ADP number (if you know it)

If the applicant is a corporate body, give the country/state of its incorporation

UNITED KINGDOM

7460272001

4. Title of the invention

DEVICE AND METHOD FOR PROCESSING A STREAM OF DATA

5. Name of your agent (if you have one)

"Address for service" in the United Kingdom to which all correspondence should be sent (including the postcode)

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DEVICE AND METHOD FOR PROCESSING A STREAM OF DATA

5 The present invention relates to a device and method for processing a stream of data. In particular, but not exclusively,
10 the device is a digital video device such as a set top box which is arranged to receive a transport stream as the stream of data.

15 Set top boxes are used, for example in the context of cable television and satellite television. A set top box is arranged to receive television programmes from a satellite or via a cable
20 and to output a programme which is displayed on a television screen or recorded on a video recorder. With both cable and satellite television, an input stream is received at an interface of the set top box. The input stream is generally scrambled and
25 comprises audio and visual information about several different television programmes, the information being time multiplexed together. Control information will also be included in the received input stream. Information relating to a television programme selected by the user is demultiplexed by the set top
30 box from the input stream to provide the selected programme which is then output by the set top box to for example a television screen, video recorder or indeed any other type of recorder.

It has been proposed to output a copy or a modified version of
35 the input stream via a further output interface. This copy or modified version of the input stream can be sent to another
40 device capable of processing that stream.

In the current proposals, the copy or modified version of the
35 input stream will include the data from the programmes of interest. Thus for a packet of the input stream, only some of the bytes of the data of the packet may be related to a programme of
40 interest and be output via the further interface. The required bytes of the packet will be at the beginning of the output packet with the remaining bytes of the packet filled with an indication that those bytes are not required or are invalid bytes. The data

5 of the bytes which are not required is discarded and is not output via the further interface.

10 This has the disadvantage that the relative timing of the data bytes relating to a required programme in the output stream will differ from that of the input stream even if the packet start timing is the same for the input and output streams. In other words, the relative timing of the bytes within the packet will differ.

15 It has been appreciated by the inventor that this may be undesirable. A processor connected to the further interface may be unable to process correctly the bytes because the relative timing of the desired bytes has changed. Additionally, the processor connected to the further interface may not be able to
20 process the data bytes efficiently because all of the desired data bytes are bunched together instead of being distributed over the whole of the data packet.

25 Accordingly, it is an aim of certain embodiments of the present invention that this problem be addressed.

30 According to one aspect of the present invention there is provided a device for receiving a stream of data, said device comprising means for selecting a plurality of portions of data from said stream of data to be output from said device; determining means for determining the relative timing of said
~~plurality of portions of data; and output means for outputting~~
the selected data, wherein the plurality of portions of data output by said output means have the same relative positions as
35 the plurality of portions of data in the received stream of data.

As the timing between the input and output data is maintained, the problems of the prior art can be circumvented.

40 The stream of data may comprise a plurality of data packets and the plurality of portions of data may occur within a packet. Each

5 portion of data may comprise a byte of data.

Means are preferably provided for identifying which of a plurality of data packets comprise data to be output by the output means. Storage means may be provided for storing
10 information for each portion of a packet indicating if that portion of data is to be output from said output means. This information may be a data portion valid signal, for example a byte valid signal. The storage means may be a first-in first-out buffer.

15 Each data packet may include information identifying the beginning of said packet and means may be provided for identifying the beginning of each packet. The means for identifying the beginning of a packet may provide an output for
20 controlling the timing of the output of the selected data by said output means. In this way, a relationship between the timing of the input data and the output data can be maintained. Preferably, a fixed latency is provided between the input plurality of portions of data received by the device and the output of those
25 selected portions of data.

Means may be provided for storing the selected portions of data. That means may be in the form of a FIFO. The means for storing the selected portions of data preferably only store the selected
30 portions of data, the other portions of data being discarded.

35 The output means may comprise a state machine which controls the output of the selected portions of data. The state machine may receive outputs from the means for storing said selected portions of data, the means for identifying the beginning of a packet and the means for storing information on each packet of data.

40 The input stream may conform to the MPEG-2 standard. The device as described hereinbefore may be incorporated in a set top box.

According to a second aspect of the present invention, there is

5 provided a method of processing a stream of data comprising the
steps of receiving a stream of data; selecting a plurality of
portions of data from said stream of data to be output;
determining the relative timing of said plurality of portions of
10 portions of data output have the same relative positions as the
plurality of portions of data in the received stream of data.

For a better understanding of the present invention and as to how
the same may be carried into effect, reference will now be made
15 by way of example to the accompanying drawings in which:-

Figure 1 schematically shows a transport stream;
Figure 2 shows a schematic diagram of a programmable transport
interface embodying the present invention;
20 Figure 3 shows a block diagram of part of the input interface and
part of the transport controller of the programmable transport
interface shown in Figure 2; and
Figure 4 shows a set top box incorporating the programmable
transport interface of Figure 2 and which is connected to a
25 recorder and a screen.

Figure 1 illustrates a portion of the transport stream 1 (data
stream) which is composed of a series of N transport packets 2.
Each transport packet 2 comprises a transport packet header 4 and
30 a transport packet payload 6. The transport stream is a bit
stream which carries in the transport packet payloads 6 of
~~information for recreating, for example, a number of different~~
television programmes. The transport stream is formed by source
encoding the television programmes. The transport stream is then
35 typically channel encoded for transmission for example by
satellite or cable and channel decoded at a respective receiver
to reproduce the transport stream. The transport stream is then
source decoded to recreate a selected one of the different
television programmes transmitted by the transport stream 1.

40

Each particular television programme may require four different

5 types of information in order to recreate the programme. That
information may consist of audio information, video information,
descrambling information and tables of programme information.
Each transport packet 2 is associated with one or more than one
10 television programme. The individual transport packets are time
division multiplexed to form the transport stream and allow the
real-time recreation of any of the different television
programmes from the transport stream.

15 To recreate a television programme, the transport stream 1 is
demultiplexed to recover only the transport payloads 6 of audio
information, video information, descrambling information and
tables of programme information which are associated with a
selected television programme. The recovered payloads are then
20 decoded to recreate the television programme. In general, only
the payloads will be scrambled and not the headers.

According to one digital broadcasting standard DVB (digital video
broadcasting) each of the transport packets is 188 bytes long of
which the transport packet header is four bytes long. The payload
25 6 contains packetising information in the form of 184 bytes.
These latter bytes contain, for example, information for
recreating a number of different television programmes as
discussed hereinbefore. With this known standard, the audio and
visual information in the payloads 6 have been packetised and
30 encoded in accordance with the MPEG-2 compression standard. A
programmable transport interface 10 (PTI), which is illustrated
in Figure 2 is used to process the received transport stream 1
and produce a data output stream 506 suitable for reconstitution
as a television programme after MPEG-2 decoding by MPEG-decoders
35 702 (see Figure 4). The programmable transport interface 10 is
included in a receiver or set top box 701 which receives the
transport stream 1.

40 The transport packet header 4 contains a synchronisation byte
which identifies the beginning of each transport packet 2. The
transport packet header 4 also contains a packet identification

5 PID which identifies the information type(s) and the television
programme(s) associated with the transport packet payload 6. The
transport packet 2 also contains information identifying the
source encoding type(s) of the transport packet. The transport
packet header 4 including the synchronisation byte and the PID
10 is not scrambled. The transport packet payload 6 may itself be
scrambled.

The programmable transport interface 10 shown in Figure 2 also
produces an alternative output stream 106 which will be described
15 in more detail hereinafter. This alternative output stream 106
may be an output derived from the transport stream. The
alternative output stream contains a portion of the transport
stream 1. This portion may be unmodified or may have been
modified for example by encryption or by changing the
20 communication standard or protocol under which the transport
stream has been prepared.

The programmable transport interface PTI 10 performs the
following functions amongst others. The PTI 10 uses the
25 synchronisation byte to identify the start of a transport packet
2 and uses the packet identification PID to identify the type(s)
of information contained in the packet and the television
programme(s) it represents. The PTI 10 descrambles if necessary,
the transport packet payload 6 and demultiplexes the transport
30 stream 1 to produce the data output stream 506, this data output
stream comprising a stream of audio information associated with
the selected television programme, a stream of video information
associated with the selected television programme and tables of
programme information associated with the selected television
35 programme. The PTI 10 then outputs these streams to the necessary
decoders 702 (Figure 4) and/or to buffers in an external memory
(not shown) to reproduce the selected television programme.

The PTI 10 comprises six functional blocks: the input interface
40 100; the transport controller 200; the instruction SRAMs (static
random access memory) 300; the data SRAM 400; the multichannel

5 DMA (direct memory access) 500; and the controller and status
register interface 600. The input interface has a transport
stream input interface 102 for receiving the transport stream 1
and an alternative stream output interface 104 for outputting the
alternative output stream 106. The function of the interface 100
10 will be described in more detail hereinafter.

The transport controller 200 receives from the input interface
100 via interconnect 108 the transport packet header 4 of the
transport packet arriving at the transport stream input interface
15 102. The transport controller 200 uses the packet identification
PID in the transport packet header 4 to determine whether the
transport packet 2 entering the input interface 100 via the
transport stream input interface 102 is associated with the
selected television programme. If it is not, the received
20 transport packet 2 is discarded. If it is, the transport
controller 200 controls the input interface 100 to descramble and
supply the transport packet payload 6 via the interconnect 108
to the transport controller 200. The transport controller 200 may
pass the payload 6 associated with audio or video information for
25 the selected programme straight to the multi-channel DMA 500 via
the interconnect 502. Alternatively, part of the payload 6 may
be output, possibly after processing by the transport controller
200, via the alternative stream output interface 104. This will
be discussed in more detail hereinafter.

30 The transport controller 200 comprises a processor in the form
of a transport controller core 124 (see Figure 3) which reads
instructions from the instruction SRAM 300. The transport
controller 200 is connected to the SRAM 300 by interconnect 304
and reads instructions from the SRAM 300 via the interconnect
35 304. A system processor 700 (see Figure 4) may read and write to
the instruction SRAM 300 via the interface 302 allowing the
transport controller instructions to be varied.

40 The data SRAM 400 can be read from and written to by the
transport controller core 124 of the transport controller 200 via

5 the interconnect 404. A search engine (not shown) within the
 transport controller 200 reads from the data SRAM 400 via
 interconnect 406. The search engine associates a pointer with
 each of the programme identification PIDs in the transport packet
 10 headers 4. The data SRAM 400 stores, at a location indicated by
 the pointer, information associated with the transport packet 2
 having a particular PID. This information is read over
 interconnect 406 and it enables the transport controller to
 control the production of input interface control signals 112 and
 the processing of the bits received on interconnect 108. The data
 15 SRAM 400 can be written to and read from the system processor 700
 via the interface 402. The transport controller 200 produces a
 transport controller output which is supplied to the multichannel
 DMA 500 via interconnect 502. The multichannel DMA 500 has an
 external memory interface 504 which supplies the data output
 20 stream 506 to decoders 702 or an external memory.

Reference will now be made to Figure 3 which shows part of the
 input interface 100 and part of the transport controller 200 in
 more detail. The input interface 100 is arranged to receive the
 25 transport stream 1 via transport stream interface 102. The input
 interface 102 also receives a byte clock 3. The transport stream
 received via transport interface 102 is passed to a packet start
 block 120. The packet start block 120 is arranged to look for the
 synchronisation byte of each transport packet 2 which identifies
 30 the beginning of each packet. In the start-up mode, the packet
 start block 120 looks at the input stream until it finds a
 synchronisation byte. In order to establish that what is located
 is a synchronisation byte and not, for example, part of the
 payload 6 which happens to contain a sequence of bits identical
 35 to that of the synchronisation byte, the packet start block 120
 checks to see that a synchronisation byte is present a
 predetermined number of bytes later, i.e. at a location
 corresponding to the beginning of the next packet.

40 In this embodiment, the packet start block 120 only checks for
 the occurrence of two synchronisation bytes spaced apart by a

5 predetermined number of bytes corresponding to the length of the packet. However, in other embodiments of the present invention, the packet start block 120 can check that the synchronisation
10 byte occurs a predetermined number of times, each occurrence of the synchronisation byte being separated by the number of bytes contained in each transport packet. For example, in the DVB standard, the packet start block would check to see that a synchronisation byte occurs every 188 bytes in order to confirm that the beginning of the transport packet has been identified. Once the packet start block 120 has verified that the beginning
15 of a transport packet has occurred, the packet start block 120 provides an output via interconnect 162 to the transport controller core 120 indicative that the beginning of a transport packet has occurred.

20 A first-in-first-out buffer FIFO 122 is connected to the output of the packet start block 120 and whilst the packet start block 120 is in the set up mode, the FIFO 122 is controlled by the transport controller core 124 via interconnect 160 to simply allow the input transport stream to flow through that FIFO 122.
25 The output of that FIFO 122 is connected to a multiplexer 126 which receives a control signal from the transport controller core 124 via interconnect 164. That multiplexer 126, in the set up mode, is arranged to pass the output of the FIFO 122 therethrough to a retiming buffer 128, which is controlled by the
30 transport controller core 124 via interconnect 166. In the set up mode of operation, the retiming buffer 128 simply outputs the transport stream received from the multiplexer 120 to the transport controller 200. In particular, the transport stream is passed by an input register 130 of the transport controller 200
35 to the transport controller core 124. Until the transport controller core 124 receives the packet start signal from the packet start block 120, the transport controller core 124 simply discards the received transport stream.

40 When the transport controller core 124 receives the signal from the packet start block 120 indicating that the beginning of the

5 packet has been located, the transport controller core 124 provides an output signal via interconnect 160 to the FIFO 122. This control signal is such that once the transport packet header 4 has passed through the FIFO 122, the FIFO 122 is prevented from passing any more of the received transport stream therethrough.
10 Instead, the payload 6 starts to accumulate in the FIFO 122. The transport packet header 4 is passed through the multiplexer 126 and the retiming buffer 128 to the transport controller 200. In particular, the transport packet header 4 is passed via the input register 130 to the transport controller core 124 which is
15 arranged to process this header. The packet header 4 may contain information which can be used to process, if necessary, the transport packet payload.

The synchronisation byte is used to control the timing of the
20 programmable transport interface 10. The transport packet header 4 also contains information as to whether or not the transport packet payload 6 is scrambled or not. If the payload 6 is scrambled, then the packet header 4 contains information about which key to use the descrambling of the payload 6. The packet
25 header 4 also contains a packet identification PID which identifies the information type(s) contained in the payload 6 and the television programme(s) carried by the associated payload 6.

The transport controller core 124 checks the transport packet
30 header 4 to determine if the payload 6 contains information on a selected television programme. This selected television programme may be a programme to be provided by interconnect 502 to the multichannel DMA 500 for viewing by the user, for example. The selected programme may be that which is to be output via the
35 alternative stream output interface 104 of the input interface 100. In embodiments of the present invention, the alternative output stream 106 may contain the same programme or a different programme to that output via the interconnect 502. This will be described in more detail hereinafter.

40 If the transport controller core 124 determines from the packet

5 header that the payload relates to a selected programme, the
transport controller core 124 determines from the header whether
or not the payload requires descrambling. If it is determined
that the payload is scrambled, then the transport controller core
10 124 is arranged to provide an output via interconnect 168 to the
descrambler 132 of the input interface 100 including at least
part of the necessary descramble key. The descramble key may be
obtained from one or more of the following: smart card (not
shown); the data SRAM via the transport controller core; and the
packet header.

15 Once a transport controller core 124 has completed the processing
of the packet header for a transport packet 1 which contains a
payload 6 relating to a selected programme, the transport
controller core 124 provides an output signal to the FIFO 122
20 allowing the accumulator payload 6 to be output therefrom. The
FIFO 122 in fact outputs the data stream both to the descrambler
132 and the multiplexer 126 directly. If the payload contains
unscrambled data, then the descrambler 132 will not be enabled
by the transport controller core 124 and the multiplexer 126 will
25 be arranged to output the data directly received from the FIFO
122. Alternatively, if the transport controller core 124 has
determined that the payload is scrambled, the descrambler 132
will be enabled. The descrambler 132 will descramble in
accordance with the descramble key, at least partially, the
30 received payload and output the descrambled payload to the
multiplexer 126. In these circumstances, the multiplexer 126 is
controlled by the transport controller core 124 via interconnect
164 to select the output from the descrambler 132 as its output.

35 The output of the multiplexer 126 is output to the retiming
buffer 128 which is controlled by the transport controller core
124 via interconnect 166. The retiming buffer 128 is in fact
another FIFO and is used to achieve smooth flow control for the
system as a whole. The retiming buffer 128 may be controlled by
40 the transport controller core 124 to store the data received from
the multiplexer 126 until a predetermined number of bits or bytes

5 have been stored in the retiming buffer 128. When the number of
bits or bytes in the retiming buffer 128 has reached the
predetermined level, then those bytes which may be output to the
transport controller 200. The function of the retiming buffer 128
is two fold. Firstly, the retiming buffer 128 stores the data
10 until such a time that the transport controller core 124 is able
to receive that data. This means that the descrambler 132 can
continue to descramble even if the transport controller is not
ready to receive the next byte of data. Secondly, the retiming
buffer is arranged to accumulate the data until the number of
15 bits of bytes has reached a predetermined level. In some
embodiments, optimum efficiency in the device is achieved if a
given minimum number of bits or bytes is dealt with by the
transport controller core 124 at the same time.

20 The payload in the retiming buffer 128 will be output to the
input register 130 of the transport controller and then to the
transport controller core 12.

25 If the transport controller core 124 determines that the data
packet contains data relating to an unselected programme, then
this packet will be discarded. The transport controller core 124
controls the FIFO 122 so that once the header of the next packet
is passed through, the FIFO 122 starts to accumulate the payload
6 at the next packet.

30 Generally, the alternative output stream 106 provided by the
input interface 100 will only relate to one programme carried by
the transport stream. However, it should be appreciated that some
embodiments of the present invention, more than one programme may
35 be output from the alternative output interface 104.

40 The transport controller core 124 is arranged to check, as
previously described, each transport packet header in order to
identify whether or not the given packet contains information
relating to the or a selected programme to be output via the
alternative output 104.

5 When it is determined that the input packet contains information
relating to a programme to be output on the alternative output
10 104, a second FIFO 103 is used to record whether each byte clock
edge contains valid data to be output via the output interface
104. When the clock edge of the byte clock is associated with
valid data, a high (or low) bit is stored as the byte valid
signal. If the clock edge of the signal is not associated with
valid data, a low (high) value is stored as the byte valid
signal. The byte valid signal is one bit for each byte. Valid
data is data to be output by the alternative output. Thus, a high
15 byte clock valid bit is stored in the second FIFO 103 for each
valid clock edge. If, on the other hand, the byte is invalid,
then an invalid indication (that is a low byte clock valid bit)
is stored in the second FIFO 103. The second FIFO 103 thus stores
the byte clock valid information which indicates if the
20 corresponding byte is valid or not. The FIFO 103 thus records
timing information on the input signal. The FIFO 103 does not
store the input data itself. The output of the second FIFO 103
is input to a state machine 107 which will be discussed in more
detail hereinafter. Thus, on each byte clock edge, the byte valid
25 signal is written into the second FIFO 103.

The packet start block 120 has a further output which is input
to a latency block 142. Each time the packet start block 120
identifies the synchronisation byte, an output is provided to the
30 latency block 142 which in turn provides an output to the state
machine 107. The output of the latency block 142 effectively acts
as a clock signal for the output of the data via the alternative
output interface 104 so that a relationship between the timing
of the input packet received via input 102 and the output packet
35 output via output interface 104 can be maintained.

The output of the first FIFO 122 is also input to a second
multiplexer 129. This second multiplexer 129 receives a second
output from the descrambler 132. Depending on whether or not the
40 programme to be output via the alternative output interface 104
is scrambled or not, the output of the FIFO 122 or the

5 descrambler 132 is selected as the output of the second
multiplexer 129. The second multiplexer has a third input from
a transport controller data unit 133. This unit 133 can receive
data or information to be output via the alternative output from
the transport controller core. The output of the data unit can
10 therefore also be selected as an output of the second multiplexer
129. The control of the multiplexer 129 is achieved by
interconnect 131 from the transport controller core 124. The
output of the second multiplexer 129 is input to a third FIFO 133
which stores the bytes to be output. It should be appreciated
15 that at this stage, the third FIFO 133 will only be storing the
bytes which are to be output via the output interface 104. Bytes
associated with the invalid byte clock bit will not be stored in
the third FIFO. Rather only bytes associated with the high valid
byte clock bits will be stored.

20 The state machine 107, as mentioned hereinbefore receives the
outputs from the second FIFO 103 and the output from the latency
block 142. The state machine may be arranged to start providing
the output of bytes from a particular packet when the next packet
25 is being received. In other words, there may be a delay of one
packet between the input and output of the desired data. However,
in alternative embodiments of the present invention, it is
possible that the delay between the input and output of data may
be less than one packet. Using the information from the second
30 FIFO 103, the state machine 107 takes the first byte from the
third FIFO 133 if the byte clock valid bit is high. That byte is
output on the state machine 107. If the first byte clock valid
bit is low, then the dummy output is provided with the low byte
clock valid output. The first byte from the third FIFO 133 will
35 only be output when a high valid bit is received from the second
FIFO 103. This is repeated for each byte stored in the third FIFO
133. Accordingly, the output provided by the output interface 104
will consist of the bytes relating to the selected TV programme
with those bytes being located in the same position within a
40 packet as in the incoming stream of data. The output may, but not
necessarily also include the byte clock valid signal information.

5 Invalid bytes may be represented by a series of zeros, a series of 1 or any other combination of bits which indicate that the byte is not valid.

10 It should be appreciated that relative timing between the bytes of data received from the input interface 102 and the alternative output 104 is thus maintained.

15 In embodiments of the invention, the third FIFO 133 may be empty but the second FIFO 103 still has low byte valid signals stored therein. Dummy data will continue to be output from the alternative output with the low byte valid signals.

20 Reference will be made to Figure 4 which shows schematically a set top box 701 which includes a programmable transport interface 10, as shown in Figure 2. The output of the programmable transport interface 10 is connected to the MPEG-2 decoder 702. The MPEG-2 decoder 702 forms part of the set top box 701. The output of the MPEG-2 decoder provides an output of the set top box 701 and is connected, for example, to a display 704. The
25 alternative output 104 of the PTI 10 is connected to a recorder 706 which may record the output data stream. For completeness sake, the channel decoder 708 of the set top box 701 is also shown. The output of the channel decoder 708 provides the input to the input interface 102 of the programmable transport
30 interface 10. The MPEG-2 decoder 702 and the programmable transport interface 10 together define the source decoder. As mentioned hereinbefore, the system processor 700 is able to vary the instructions for the transport controller of the programmable interface.

35 It is preferred that real time processing of the input stream occur to provide the alternative output stream. However, in some embodiments of the present invention, there may be a delay therebetween. It is also preferred that there be a fixed latency
40 between the input stream 1 of the input interface 100 and the alternative stream 106 of the input interface 100.

5 The alternative stream output may be connected to a recorder.
However, the alternative stream output can be connected to any
other suitable device such as a screen, a digital video recorder,
a PC, another set top box, a network connector or the like. The
10 alternative stream output may be connected to an IEEE-1394
interface.

Whilst embodiments of the present invention have been described
in the context of an MPEG system, embodiments of the present
invention can be used with other systems.

15 In embodiments of the present invention, the alternative output
may have some encryption. However, the relative timing between
the input bytes of data from the input interface and the bytes
output by said alternative output is retained.

20 It should be appreciated that embodiments of the present
invention can be used in applications other than set top boxes.
For examples, the PTI may be included in an ATM receiver or the
like. Embodiments of the present invention may be applied to any
25 suitable digital video device. Embodiments of the present
invention are particularly applicable to consumer digital goods
such as digital television or the like. Embodiments of the
invention can be used with conditional access modules. In
particular, conditional access modules can be added to a generic
30 digital video system to customise it to receive a broadcasters
(or other type of service providers) signals, descramble and
decode. Embodiments of the invention can be used to process the
transport stream and descramble it in a conditional access
module.

35

CLAIMS:

1. A device for receiving a stream of data, said device comprising:

means for selecting a plurality of portions of data from said stream of data to be output from said device;

determining means for determining the relative timing of said plurality of portions of data; and

output means for outputting the selected data, wherein the plurality of portions of data output by said output means have the same relative positions as the plurality of portions of data in the received stream of data.

2. A device as claimed in claim 1, wherein said stream of data comprises a plurality of data packets and said plurality of portions of data occur within a packet.

3. A device as claimed in claim 2, wherein each portion of data comprises a byte of data.

4. A device as claimed in claim 2 or 3, wherein means are provided for identifying which of said plurality of data packets comprise data to be output by said output means.

5. A device as claimed in any preceding claim, wherein storage means are provided for storing information for each portion of a packet indicating if the portion of data is valid or invalid.

6. A device as claimed in claim 5, wherein said information comprises a data portion valid signal.

7. A device as claimed in claim 5 or 6, wherein the storage means comprises a first-in-first-out buffer.

8. A device as claimed in any one of claims 2 to 7, wherein each data packet includes information identifying the beginning

5 of said packet and means are provided for identifying the beginning of each packet.

9. A device as claimed in claim 8, wherein said means for identifying the beginning of a packet provides an output for
10 controlling the timing of the output of the selected data by said output means.

10. A device as claimed in claim 9, wherein a fixed latency is provided between the input plurality of portions of data
15 received by the device and the output of those selected portions of data.

11. A device as claimed in any one of the preceding claims, wherein means are provided for storing the selected portions of
20 said data.

12. A device as claimed in claim 11, wherein the means for storing the selected portions of data stores only the selected
25 portions of data.

13. A device as claimed in claim 11 or 12, wherein the means for storing the selected portions of data is a first in first out
buffer.

14. A device as claimed in any of claim 11 to 14 when appended to any of claims 4 to 7 and any of claims 8 to 10, wherein the
30 output means comprises a state machine which controls the output of the selected portions of data, said state machine receives
outputs from said means for storing said selected portions of data, and said means for storing information on each portion of
35 data.

15. A device as claimed in any preceding claim, wherein the input stream conforms to the MPEG-2 standard.

16. A digital video device incorporating a device as claimed in
40

5 any one of the preceding claims.

17. A method of processing a stream of data comprising the steps of:

receiving a stream of data;

10 selecting a plurality of portions of data from said stream of data to be output;

determining the relative timing of said plurality of portions of data; and

15 outputting the selected data, wherein the plurality of portions of data output have the same relative positions as the plurality of portions of data in the received stream of data.

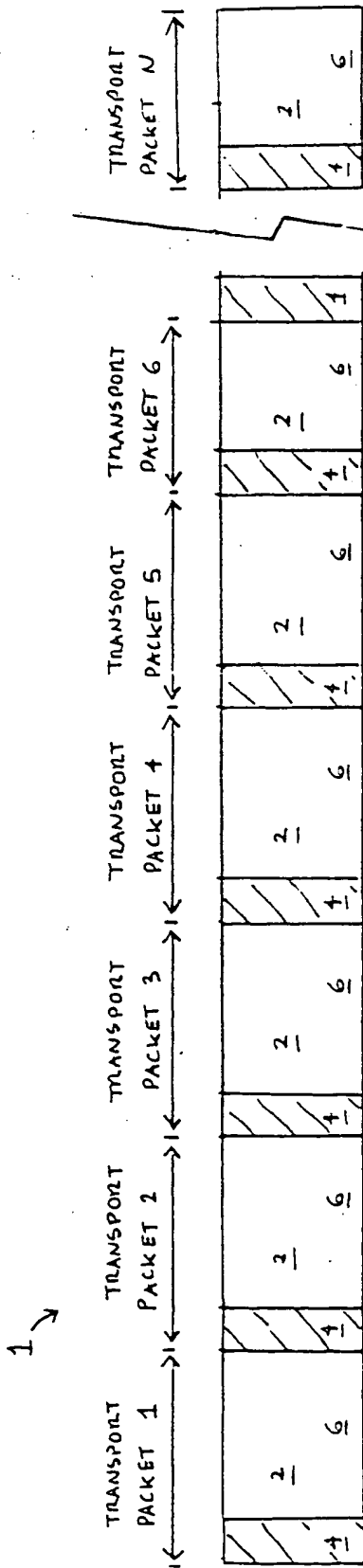


Fig. 1

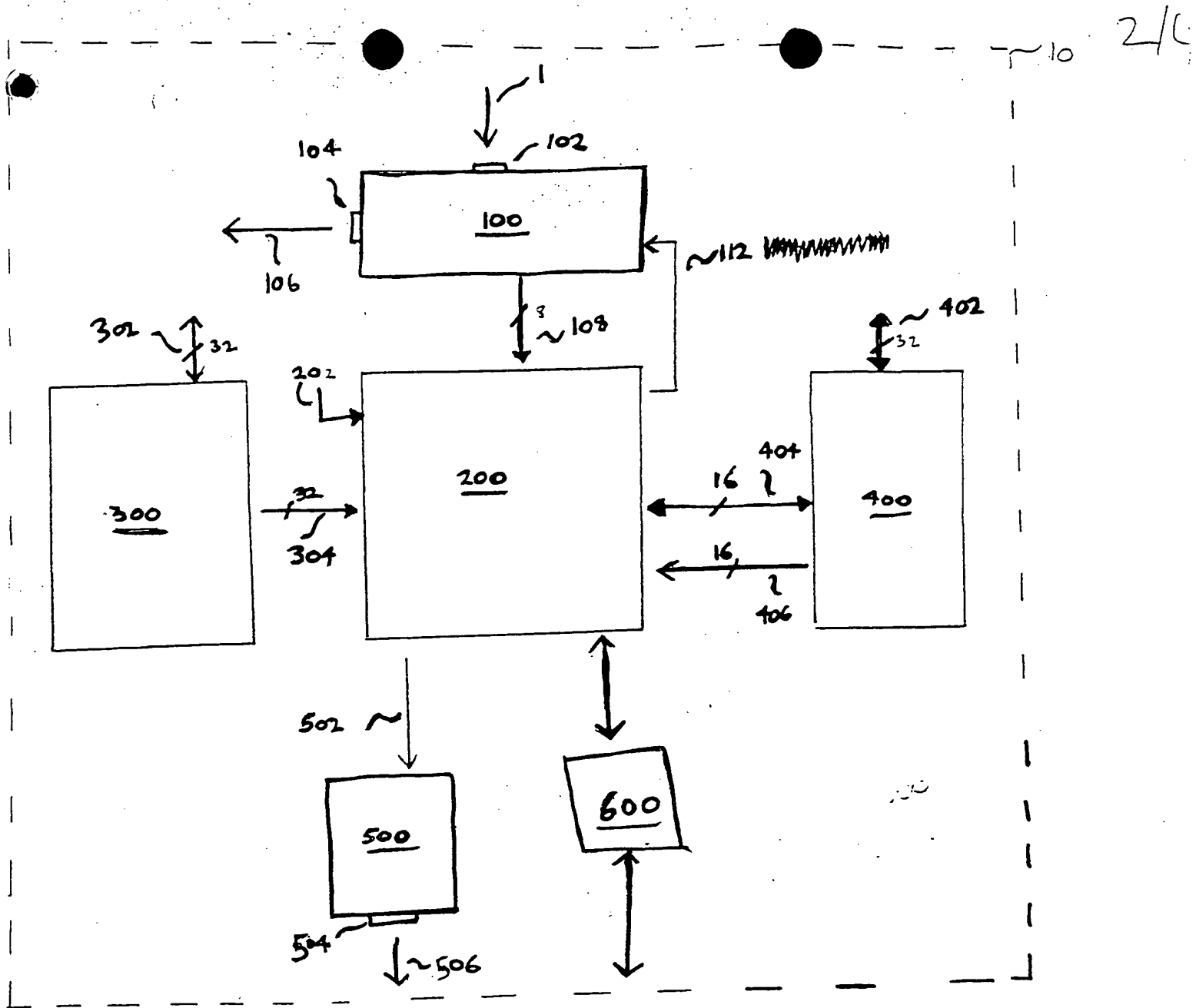


Fig. 2

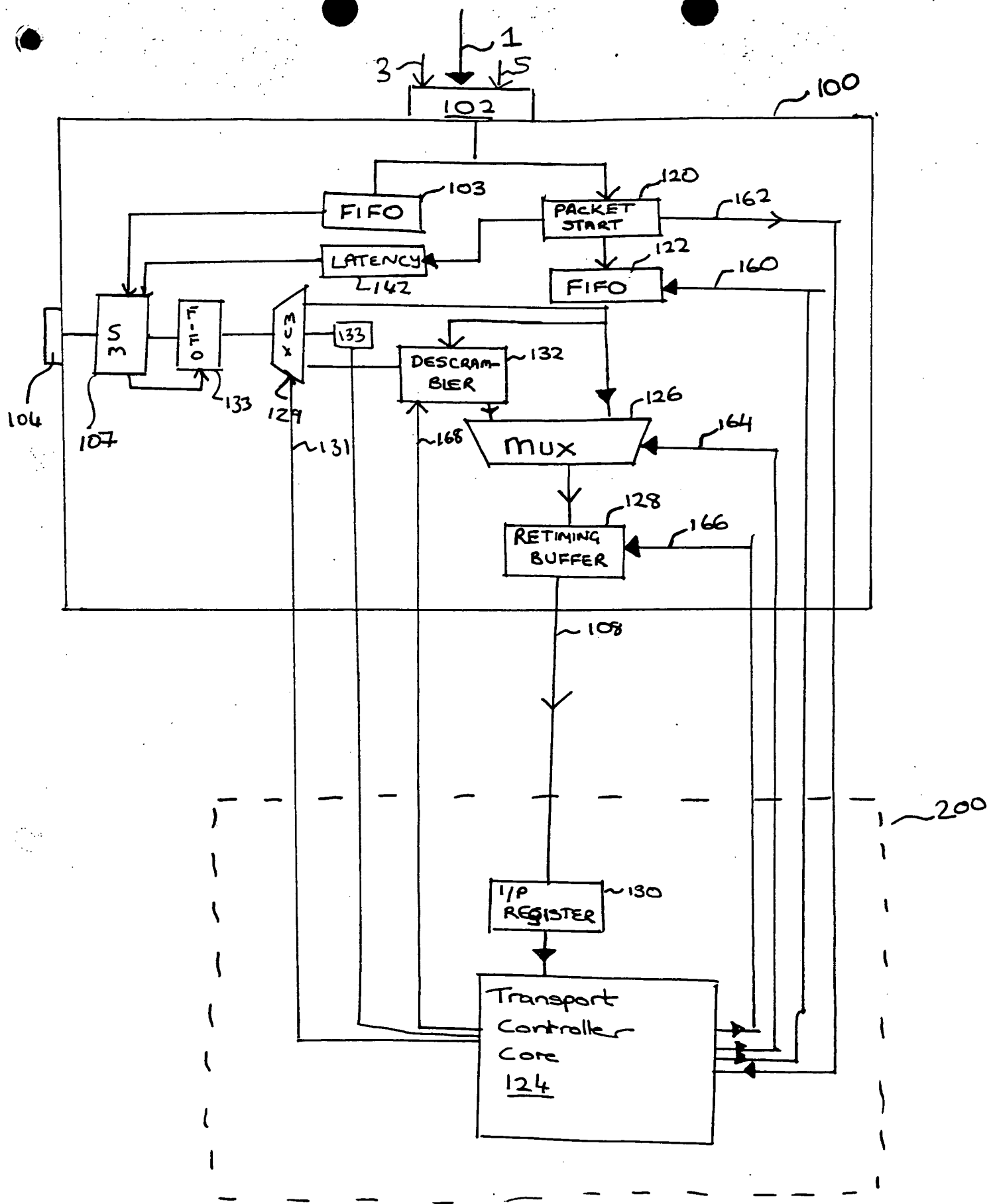


FIGURE 3

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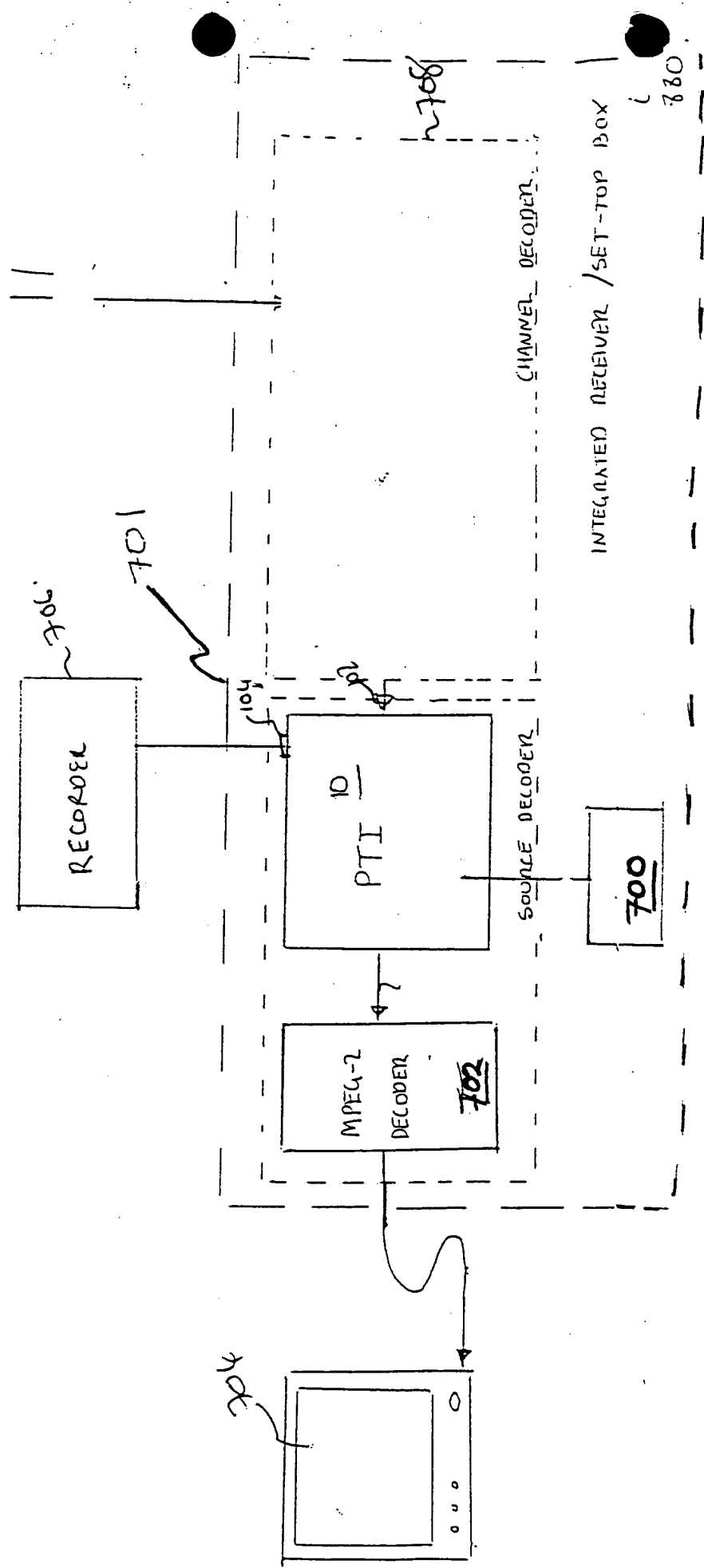


FIGURE 4

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